REMARKS

A. Status of the Claims

Claims 1-62 are pending in the application. Claims 1-6 are withdrawn. Claims 26 and 27 were rejected under 35 USC 112, second paragraph. Claims 7, 11-13, 17, 22-23, 26-27, 30, 32, 34-35, 43-46, and 62 were rejected under 35 USC 102(b) as being anticipated by Park et al., US Patent No. 6,727,514. Claims 8-10, 18-21, 24, 25, 31, 36-40, 42, 47-49, 53-59, and 61 were rejected under 35 USC 103(a) as being unpatentable over Park et al. in view of Yonehara, US Patent No. 5,457,058.

Claims 14-16, 28-29, 33, and 50-52 were rejected under 35 USC 103(a) as being unpatentable over Park et al. in view of Lin, US Patent Pub. No. 2004/0235276. Claim 41 was rejected under 35 USC 103(a) as being unpatentable over Park et al. in view of Yonehara and further in view of Lin.

B. 35 USC 112 Rejections: Claims 26 and 27

Claims 26 and 27 were rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which Applicants regard as the invention.

The Examiner pointed out that claim 24 recites that the crystallizing agent is silicon, while claim 26, which depends from claim 24, recites that the crystallizing agent is germanium. The Examiner has correctly noted that this is illogical and thus indefinite, and Applicants appreciate identification of this error. Claim 26 was intended to depend from claim 22, and has been so amended in this response.

C. 35 USC 102(b) Rejections: Claims 7, 11-13, 17, 22-23, 26-27, 30, 32, 34-35, 43-46, and 62

Claims 7, 11-13, 17, 22-23, 26-27, 30, 32, 34-35, 43-46, and 62 were rejected under 35 USC 102(b) as being anticipated by Park et al.

Claims 7, 11-13, 30, 32, and 43-46 have been cancelled.

Claim 17 has been amended to depend from claim 8. The rejection of claim 8 willl be discussed in Section D of these remarks.

Claim 22 recites a method for producing a wafer having a crystallized silicon layer with controlled defect density, the method comprising: forming a first layer of amorphous silicon on the wafer; selectively introducing a crystallizing agent on the amorphous silicon layer in a substantially symmetric pattern across a seeded area; and annealing the amorphous silicon layer, wherein, after the annealing step, in the seeded area, an area bounded by adjacent nucleation sites encloses no more than five crystal grain boundaries.

The Examiner points to Figs. 1(c) and 1(d) as evidence that the area bounded by adjacent nucleation sites encloses no more than five crystal grain boundaries. It is true that in Fig. 1(c) only four grain boundaries are shown in the area bounded by any four adjacent nucleation sites. This is because only the crystallized regions 107 surrounding each nucleation site are of interest to Park et al., and only the grain boundaries of crystallized regions 107 are shown.

Applicants will maintain, however, that, referring to Fig. 1(c), one skilled in the art will appreciate that region 111, between crystallized regions 107, will have multiple grain boundaries which are not shown. As Park et al. describe (col. 7, lines 58-62),

regions 111 are either amorphous or polycrystalline. In either case, there will be multiple additional grain boundaries in each of these regions. These grain boundaries are not shown because they are not important to the invention of Park et al., as Park et al. only teaches formation of TFTs within the boundaries of crystallized regions 107, as in Figs. 4(a) and 6(a) of Park et al.

As described in paragraphs [0062] and [0063] and accompanying Figs. 4a and 4b of the present application, the only way to guarantee that there will be no more than five grain boundaries in the area bounded by adjacent nucleation sites is to continue crystallization until the grain boundaries of adjacent crystallized regions meet, leaving no region like amorphous or polycrystalline region 111 of Park et al. There is no teaching in Park et al., however, that crystallization continues until the *entire* amorphous silicon layer is included in crystallized regions 107; in fact Park specifically shows and refers to regions 111 *between* and not included in crystallized regions 107. Thus there will be more than five grain boundaries in the area of Park et al. bounded by adjacent nucleation sites.

Claims 34 and 35 have been amended to depend from claim 31. The rejection of claim 31 is discussed in Section D of these remarks.

Claim 62 recites a method for controlling grain boundaries in a polysilicon layer, the method comprising: forming a first amorphous silicon layer on a wafer, forming a mask layer on and in contact with the first amorphous silicon layer; etching the mask layer wherein portions of the amorphous silicon layer are exposed; depositing ***silicon nuclei*** on the mask layer and on the first amorphous silicon layer; forming a second

amorphous silicon layer in contact with at least portions of the first amorphous silicon layer, and annealing the wafer.

Applicant respectfully points out that, while Park et al. teach the use of various crystallization accelerating materials, including Ge, Ni, and other materials named at col. 6, lines 32-40, Park et al. do not teach use of silicon nuclei as the crystallizing agent.

Applicants have shown that Park et al. do not teach each and every limitation of claims 22-23, 26-27, and 62, and thus respectfully request that the 102(b) rejection of these claims be withdrawn. Claims 7, 11-13, 30, 32, and 43-46 were cancelled, while claims 17, 34, and 35 were amended to depend from claims rejected under different rationales.

D. 35 USC 103(a) Rejections: Claims 8-10, 18-21, 24, 25, 31, 36-40, 42, 47-49, 53-59, and 61

Claims 8-10, 18-21, 24, 25, 31, 36-40, 42, 47-49, 53-59, and 61 were rejected under 35 USC 103(a) as being unpatentable over Park et al. in view of Yonehara.

Claim 8 has been amended to include the limitations of cancelled claim 7, from which it formerly depended. As amended, claim 8 recites a method for crystallizing a polysilicon layer on a wafer, the method comprising: forming a first amorphous silicon layer; selectively introducing a crystallizing agent on the amorphous layer in a substantially symmetric pattern in two dimensions; and annealing the wafer to form the crystallized polysilicon layer, wherein substantially no amorphous silicon remains between silicon grains in the polysilicon layer, wherein the crystallizing agent is silicon nuclei.

The Examiner finds all of these elements in Park et al. except that Park et al. does not disclose that the crystallizing agent is silicon nuclei. The Examiner finds silicon nuclei to be the crystallizing agent as taught by Yonehara, and suggests using the silicon nuclei of Yonehara in the invention of Park et al.

The techniques of Park et al. and of Yonehara, however, are fundamentally different, and could not be readily combined. Park et al. teach that the crystallization accelerating material 103 is "adhered at each of lattice points in a matrix, **upon a surface** of the amorphous crystalline thin-film semiconductor layer," (col. 4, lines 42-43), presumably by a deposition method. Crystallization accelerating material 103 is shown *on the surface* of amorphous layer 102 in Fig. 1(b). The embodiments in which crystallization accelerating material 103 is shown not on top of the amorphous layer, it is either *below* the amorphous layer 104, as in Fig. 3(a), or between *two* deposited layers 105 and 106, as in Fig. 3(b).

In contrast, all embodiments of Yonehara teach *injection* (or implantation) of silicon ions, in which the ions are injected to a depth *within* an amorphous layer (see Abstract.) In fact, Yonehara describes that the crystallization temperature depends strongly on the ion injection energy (col. 3, lines 38-39); thus the fact of the *injection* of ions within an amorphous layer is clearly central to the invention of Yonehara.

There is no teaching in Park et al. to inject the crystallization accelerating agent 103, as required by Yonehara. There is no teaching in Yonehara or Park et al. that silicon nuclei which are *not* injected will behave as effective crystallization agents; thus there is no motivation to attempt such a combination. The same rationale applies to the rejections of claims 24, 31, 39, 47, 56, and 62 and their dependent claims 25, 36, 48, 49, and 57-61.

Claim 17 has been amended to depend from claim 8 (rather than claim 7, from which it formerly depended) and thus it and its dependent claims 18-21 also distinguish over the suggested combination.

Claim 9 adds the limitations that the step of selectively introducing a crystallizing agent in a substantially symmetric pattern comprises: forming a mask layer on the first amorphous silicon layer; etching holes in the mask layer, the holes distributed in a substantially symmetric pattern and exposing portions of the first amorphous layer; and depositing silicon nuclei on the mask layer and the exposed portions of the first amorphous layer. Applicants respectfully point out that in her rejection of claim 9, the Examiner describes finding these elements in Park et al., with the exception that in Park et al., *germanium* is deposited on the mask layer rather than silicon nuclei. Though Applicant cannot find such suggestion, Applicants assume that the Examiner then intends to substitute the injected silicon ions of Yonehara for deposited germanium of Park et al. This combination cannot be made, and would not be made by one skilled in the art, as described above.

Claim 37 recites a method for maximizing grain size and controlling density of grain boundaries in crystallized silicon, the method comprising: forming a first amorphous silicon layer on a wafer; selectively creating nucleation sites at substantially uniform intervals on the first amorphous silicon layer; annealing the wafer to convert the amorphous layer to polysilicon; and forming a plurality of memory cells in the polysilicon, wherein portions of the cells comprise portions of the polysilicon, and **wherein placement of the nucleation sites and placement of individual memory cells is not coordinated.**

The Examiner declines to grant patentable weight to the limitation that memory cells are formed in the polysilicon layer, wherein placement of the nucleation sites and placement of individual memory cells is not coordinated, citing *Ex parte Pfeiffer*, and requiring that the structure limitations in this method claim must affect the method in a manipulative sense.

Applicants point out that the structure strongly affects the step of forming a plurality of memory cells. The purpose of Park et al. is to improve the quality of active devices, such as the TFTs shown fabricated in Figs. 4(a) and 6(a) in crystallized regions 107 (see col. 1, lines 46-52.) Without exception, in Park et al., the TFTs *are* coordinated with the placement of nucleation sites: The TFTs are placed entirely within crystallized region 107. The fabricated TFT may be centered on the nucleation site (as in Fig. 4(a)) when germanium is used as a crystallization acceleration material to benefit from the higher mobility when germanium is incorporated (col. 8, line 62-col. 9, line 11.) Alternatively the TFT may be placed to be within crystallized region 107 yet *avoid* the nucleation site at the center of crystallized region 107 as in Fig. 6(a) when using crystallization acceleration materials other than germanium (col. 9, lines 47-63), presumably to avoid metal contamination (col. 7, line 66-col. 8, line 6.)

The method of Park et al. makes it impossible to place memory cells without coordinating their location to the placement of nucleation sites. Thus this placement affects the formation of memory cells, a step of the method, and is entitled to patentable weight. Thus claim 37 and its dependent claims 38-42 distinguish over the suggested combination.

Applicants respectfully note that Applicants could not determine what teaching of Yonehara was relied upon in the rejection of claim 37.

Applicants note that claim 53, which was rejected using the rationale used to reject claim 37, is in fact a device claim. Applicants further note that, as in claim 37, the method step of forming the memory array, wherein the memory array comprises at least two levels of memory cells, one level formed vertically above another, is strongly influenced by the structural limitation of having no amorphous silicon remaining between the grains, as this allows the placement of memory cells anywhere within the silicon layer.

Regarding the rejection of claim 39, as noted earlier, the use of deposited silicon nuclei as the crystallizing agent is not taught or suggested in the references and thus further distinguishes over the suggested combination.

Claim 54 recites a method for producing a wafer having a crystallized silicon layer with controlled defect density, the method comprising: forming a first layer of amorphous silicon on the wafer; selectively introducing a crystallizing agent on the amorphous silicon layer in a substantially symmetric pattern across a seeded area, the seeded area having a first distance between nucleation sites; and annealing the amorphous silicon layer, wherein, after the annealing step, in the seeded area, a chance that a square area having a side less than about one fourth of the first distance has no more than one grain boundary is greater than about .75.

The Examiner finds this low density of grain boundaries in Park et al. Applicants point out that, as described in the response to the rejection of claim 22 in Section C of these remarks, there will be many grain boundaries in the area 111 shown in Fig 1(c),

which is either amorphous or polycrystalline (col. 7, lines 58-62.) Thus it *cannot* be guaranteed that an area as in the claim can have a known probability of having more than one grain boundary. Claim 54 and its dependent claims 55-61 thus distinguish over the references.

Applicants have shown that references cannot be combined, that one skilled in the art would not be motivated to combine them, and the rejected claims are neither taught nor suggested by the suggested combination, and respectfully request reconsideration of claims 8-10, 18-21, 24, 25, 31, 36-40, 42, 47-49, 53-59, and 61.

E. 35 USC 103(a) Rejections: Claims 14-16, 28-29, 33, and 50-52

Claims 14-16, 28-29, 33, and 50-52 were rejected under 35 USC 103(a) as being unpatentable over Park et al. in view of Lin.

Claim 14 has been amended to include the limitations of cancelled claim 7, from which it formerly depended. As amended, claim 14 recites a method for crystallizing a polysilicon layer on a wafer, the method comprising: forming a first amorphous silicon layer; selectively introducing a crystallizing agent on the amorphous layer in a substantially symmetric pattern in two dimensions; and annealing the wafer to form the crystallized polysilicon layer, wherein substantially no amorphous silicon remains between silicon grains in the polysilicon layer, wherein the crystallizing agent is laser energy.

The Examiner proposes using laser energy, as described by Lin, in the method of Park et al. for the purpose of increasing the grain size of the polysilicon film.

Applicants believe, however, that the methods of Lin and Park et al. cannot be combined. In Park et al., a crystallization accelerating material 103 is deposited, then

crystallization spreads *outward* from the crystallization accelerating material 103 to form a crystallized region 107 (col. 7, lines 36 42.) In contrast, paragraph [0007] and Figs. 2 and 3 of Lin describe that, using the laser method of Lin, nucleation begins at the boundary between a masked region 28 and an exposed region 26, and proceeds *inward*, crystallizing the exposed region. The addition of heat-retaining capping layer 118 of Fig. 6 of Lin limits the loss of heat, but in this embodiment as well, nucleation begins at the boundary between the masked region 130 and the exposed region 120 and proceeds *inward*, crystallizing region 122 of amorphous layer 114 of Lin (paragraph [0019].) It is not clear that the masked region 130 is crystallized at all, and this region is removed entirely and not used in device fabrication, as shown in Fig. 7 and described in paragraph [0021]. The same rationale applies to the rejections of claims 28, 33, and 50.

Applicants have shown that the references cannot be combined, and thus respectfully request reconsideration of claims 14-16, 28-29, 33, and 50-52.

F. 35 USC 103(a) Rejections: Claim 41

Claim 41 was rejected under 35 USC 103(a) as being unpatentable over Park et al. in view of Yonehara and further in view of Lin.

Claim 41 recites a method for maximizing grain size and controlling density of grain boundaries in crystallized silicon, the method comprising: forming a first amorphous silicon layer on a wafer; selectively creating nucleation sites at substantially uniform intervals on the first amorphous silicon layer; annealing the wafer to convert the amorphous layer to polysilicon; and forming a plurality of memory cells in the polysilicon, wherein portions of the cells comprise portions of the polysilicon, and wherein placement of the nucleation sites and placement of individual memory cells is

not coordinated, wherein the step of selectively creating nucleation sites at uniform intervals comprises exposing the first amorphous silicon layer to laser energy at uniform intervals. (This summary includes the limitations of claim 41 and of claim 37, from which it depends.)

The Examiner finds the limitations of claim 37 in Park et al., and modifies the teachings of Park et al. to use laser energy as in Lin. As described in Section E of these remarks, however, Applicants believe that because the crystallization front of Park et al. advances *outward*, while the crystallization front of Lin advances *inward*, these methods cannot be combined. Applicant cannot determine the relevant teaching of Yonehara and thus will not address it.

Applicants have shown that the references cannot be combined, and respectfully request consideration.

CONCLUSION

In view of the preceding Remarks, Applicants submit that this application is in condition for allowance. Reconsideration is respectfully requested. If objections remain, Applicants **respectfully request an interview.** In the event that objections remain, the Examiner is asked to contact the undersigned agent at (408) 869-2921.

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